ISA-PIO

48 Channel TTLDigital I/O Board

User Manual

ISA-PIO

User Manual

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OUTLINE DESCRIPTION

This card provides 48 programmable digital I/O channels. It is suitable for sensing the presence of or driving TTL connections only. There is provision for a set of on board pull up resistors to enable the board to be used to detect contact closures on push buttons, relay contacts etc.

1.0 SPECIFICATIONS

1.1 Electrical Specification

Number of channels	48
I/O Logic Levels ' ON'	2.4V to 5V TTL Level
Maximum I/O Voltage	5V
Power Requirement	5V D.C. @ 150mA
Power Dissipation	500mW
Max Sink Current (Output)	1.7mA @ 0.45V
Max Source Current	200uA @ 2.4V

1.2 Physical Specification

Height	107mm
Width	15mm
Depth	132mm

Electromagnetic Compatibility (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in a Blue Chip Technology Icon industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements for an industrial environment (Class A product) subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for the industrial environment.

- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.

- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.

- Most EMC problems are caused by the external cabling to the board. Boards fitted with IDC ribbon cable connectors on the metal mounting bracket require particularly careful installation of the external cabling. The cabling must be totally screened; the type of ribbon cable which is rolled to a round form with a braided wire screen is best. Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC. Keep the unscreened section as short as possible. The mounting bracket of the board includes a captive nut as an screen earth point. Connect the screen of the cable to this by the shortest possible wire.

- To ensure that the board meets the industrial radiated field immunity of 10V/metre, the cable should also be fitted with a ferrite clamp on the external cable as close as possible to the connector. The preferred type is the Chomerics clip-on-style, type H8FE-1004-AS.

- Ensure that the screen of the ribbon cable is bonded to a good RF earth at the remote end of the cable.

- Cables which connect externally to boards at TTL levels should not exceed two metres in length. This restriction does not apply to opto-isolated boards.

Failure to observe these recommendations may invalidate the EMC compliance.

Warning

This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

EMC Specification

A Blue Chip Technology Icon industrial PC fitted with this card meets the following specification:

Emissions:	EN 55022:1995	
	Radiated	Class A
	Conducted	Class A & B
Immunity:	pr EN 50082-2:1991 incorporating:	
	Electrostatic Discharge	IEC 801-2:1984 Performance Criteria A
	Radio Frequency Susceptibility	IEC 801-3:1984 Performance Criteria A
	Fast Burst Transients	IEC 801-4:1988 Performance Criteria A

2.0 USER ADJUSTMENTS

2.1 Selecting the Base Address

The board may be located in any 62 pin slot in the PC motherboard but must be set up to appear at a specified position (or ' address') in the port map. Available positions are shown in the IBM-PC Technical Reference Guide. However, for those who do not possess a copy of this document a good place is the location normally allocated to the prototyping card as supplied by IBM. This address is 300 Hex or 768 decimal.

All Blue Chip Technology cards are preset to this address at the factory. However, no two devices should be used while set to the same address since contention will occur and neither board will work. If your machine contains a card with a conflicting address then another reasonably safe address is 200 to 21F (Hex).

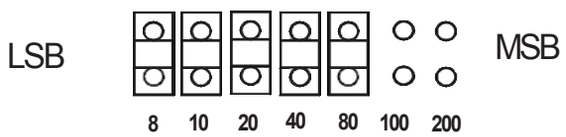
A set of links is provided on the board to set the base address of the board within the IBM-PC port map. The address is in binary with the presence of a link representing a 0 and the absence of a link representing a 1.

To set the base address to 768 Decimal (300 Hex) set the following pattern on the links as indicated below

Figure 1 - Selecting the Base Address

Note: View board with back panel on RHS.

Middle 7 bits of port address on links.



More example addresses are shown in Appendix A.

Note: No two cards must occupy the same address.

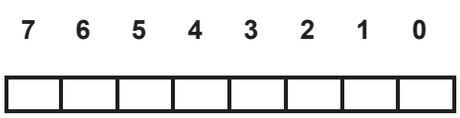
2.2 Port Map

The ISA-PIO has two 8255 chips. Each chip has three 8 bit ports which can be programmed as input or output by writing a control word to the control port. (See Table 3). Port A and B (A' and B') must be all input or all output. Port C may be split into two 4 bit sections each of which may be input or output.

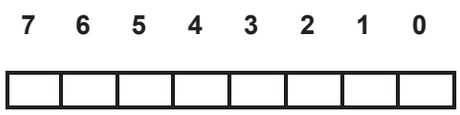
The board occupies eight read/write addresses (four for each 8255 chip) in the IBM-PC port map.

Address

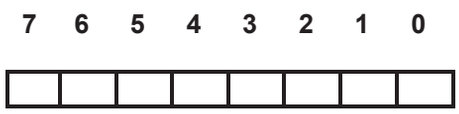
Base + 0	Port A	
Base + 1	Port B	8255 N ° 1
Base + 2	Port C	
Base + 3	Command Port	
Base + 4	Port A'	
Base + 5	Port B'	8255 N ° 2
Base + 6	Port C'	
Base + 7	Command Port	



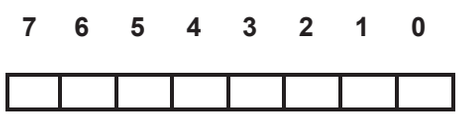
DATA
(8255 PORT A)



DATA
(8255 PORT B)



DATA
(8255 PORT C)



CONTROL

Bit 0 = Port C (Lower)	0 = Output,	1 = Input.
Bit 1 = Port B	0 = Output,	1 = Input.
Bit 2 = Mode Selection	0 = Mode 0,	1 = Mode 1.
Bit 3 = Port C (Upper)	0 = Output,	1 = Input.
Bit 4 = Port A	0 = Output,	1 = Input.
Bits 5,6 = Mode Selection	00 = Mode 0, 1X = Mode 2.	01 = Mode 1,
Bit 7 = Mode Set Flag	0 = Inactive,	1 = Active.

See Table 3 for quick set-up guide.

3.0 ELECTRICAL OPTIONS

3.1 Input conditioning

The 8255 has high impedance inputs. An option is provided to terminate external input lines. This is useful in an electrically noisy environment or where a load is required (e.g. open collector drive). The termination may be pull up (to 5V) or pull down (to 0V) via 6 SIL resistor packs (RP 2-7). Links B-G select pull up or pull down. (See circuit diagram).

3.2 Input/Output Connections

A 50 way insulation displacement connector (IDC) is provided on the PC rear panel of the board for I/O channel signal connection. If access to individual channels is required, a 50 way IDC ribbon cable may be used to connect the I/O channels to a 50 way screw terminal block available from Blue Chip Technology as part number ST-24.

The pins are numbered as shown in the following diagram. Pins 1-48 contain the I/O channels and pins 49 and 50 are connected to digital ground.

When the connector is viewed from the back of the system odd numbered pins are on the left and even numbered pins are on the right with pin 1 at the top of the connector.

Pin Detail

Pin	1	O	O	Pin	2
Pin	3	O	O	Pin	4
.		O	O	.	
.		O	O	.	
.				.	
.				.	
.				.	
.		O	O	.	
.		O	O	.	
Pin	47	O	O	Pin	48
Pin	49	O	O	Pin	50

View with gold edge connectors downwards.

3.3 Connector Pin Details

Port	Bit	Pin	Pin	Bit	Port
A	0	1 o	o 2	0	A'
	1	3 o	o 4	1	
	2	5 o	o 6	2	
	3	7 o	o 8	3	
	4	9 o	o 10	4	
	5	11 o	o 12	5	
	6	13 o	o 14	6	
	7	15 o	o 16	7	

Port	Bit	Pin	Pin	Bit	Port
B	0	17 o	o 18	0	B'
	1	19 o	o 20	1	
	2	21 o	o 22	2	
	3	23 o	o 24	3	
	4	25 o	o 26	4	
	5	27 o	o 28	5	
	6	29 o	o 30	6	
	7	31 o	o 32	7	

Port	Bit	Pin	Pin	Bit	Port
C	0	33 o	o 34	0	C'
	1	35 o	o 36	1	
	2	37 o	o 38	2	
	3	39 o	o 40	3	
	4	41 o	o 42	4	
	5	43 o	o 44	5	
	6	45 o	o 46	6	
	7	47 o	o 48	7	

Digital Ground 49 o o 50 Digital Ground

4.0 OPERATING GUIDE

4.1 Using the Device

A total of 24 I/O channel signals may be connected to each of the 8255 I/O devices on the ISA-PIO board providing 6 eight bit ports. Each signal is connected to one bit within one of these ports, i.e.

Port Add	Bit	Hex	Decimal	Port Add	Bit	Hex	Decimal
	0	01	1		0	01	1
	1	02	2		1	02	2
	2	04	4		2	04	4
	3	08	8		3	08	8
+0	4	10	1	+4	4	10	16
	5	20	32		5	20	32
	6	40	64		6	40	64
	7	80	128		7	80	128
	0	01	1		0	01	1
	1	02	2		1	02	2
	2	04	4		2	04	4
	3	08	8		3	08	8
+1	4	10	16	+5	4	10	16
	5	20	32		5	20	32
	6	40	64		6	40	64
	7	80	128		7	80	128
	0	01	1		0	01	1
	1	02	2		1	02	2
	2	04	4		2	04	4
	3	08	8		3	08	8
+2	4	10	16	+6	4	10	16
	5	20	32		5	20	32
	6	40	64		6	40	64
	7	80	128		7	80	128

4.2 Programming Guide

The state of the input lines may be determined by using either of the following methods:-

(a) Microsoft BASIC A or GW BASIC.

X=INP (P)

Returns the byte from port P and assigns this value to the variable, X.

(b) 8088/8086 Assembly language.

```
PORT  EQU 0300H

GETDAT:

        MOV     DX, PORT
        IN      AL,DX
        RET
```

The state of the output lines may be modified by using either of the following methods:-

(a) Microsoft BASIC A or GW BASIC.

OUT P, D

Outputs the byte D to port P.

(b) 8088/8086 Assembly language

```
PORT  EQU 0300H

PUTDAT:

        MOV     DX, PORT
        MOV     AX, DATA
        OUT     DX, AL
        RET
```

The following table gives a summary of the most commonly used ' control words' which must be written to the control port to configure the 8255 before using this module.

The 8255 can operate in one of 3 modes (mode 0-2).

In the first mode (mode 0) the 8255 provides simple I/O for 3, 8 bit ports. Data is simply written to or read from a specified port (A, B or C) without the use of handshaking. The following Control Code Table (3) assumes mode 0 is required.

Mode 1 enables the transfer of data to or from a specified 8 bit port (A or B) in conjunction with strobes or handshaking signals.

In mode 2 data is transferred via one bi-directional 8 bit port (A) with handshakes (Port C).

Control Word (Hex)	Control Word (Decimal)	Sets All of Port A To	Sets All of Port B To	Sets High 4 Bits of Port C To	Sets Low 4 Bits of Port C To
80	128	Output	Output	Output	Output
81	129	Output	Output	Output	Input
82	130	Output	Input	Output	Output
83	131	Output	Input	Output	Input
88	136	Output	Output	Input	Output
89	137	Output	Output	Input	Input
8A	138	Output	Input	Input	Output
8B	139	Output	Input	Input	Input
90	144	Input	Output	Output	Output
91	145	Input	Output	Output	Input
92	146	Input	Input	Output	Output
93	147	Input	Input	Output	Input
98	152	Input	Output	Input	Output
99	153	Input	Output	Input	Input
9A	154	Input	Input	Input	Output
9B	155	Input	Input	Input	Input

Table 3 - Control Word Table

4.3 Example Program

The following program in Microsoft Basic will test the operation of the ISA-PIO if a link is made between corresponding pins on the rear connector.

```
10      P1=&H300 :   REM BASE OF FIRST     PIA
15      P2 = &H304 :   REM BASE OF SECOND     PIA
20      GOSUB 60
30      P1 = &H304 : P2 = &H300
40      GOSUB 60
50      GOTO 10 :   REM LOOP   CONTINUOSLY
60      OUT P1+3, &H80 : OUT P2+3, &H9B
70      FOR P = 0 TO 2
80      F = 0
90      A = 1
100     OUT P1+P, A
110     IF  INP (P2+P)<>A THEN PRINT      ″ERROR ″, P, A,   INP
        (P2+P) : F=F+1
120     A=A+A
130     IF A=256 THEN    GOTO 150
140     GOTO 100
150     IF F>0 THEN PRINT P,     ″FAILED ″, F :  GOTO 170
160     PRINT P,   ″PASSED ″
170     NEXT P
180     RETURN
```

The above program runs continuously and can only be stopped by pressing control and break on the PC keyboard.

5.0 COMMERCIAL DATA ACQUISITION PACKAGES

The Blue Chip Technology ISA-PIO can be used with almost any data acquisition package that can read information directly from a PC input port.

5.1 Use of the ISA-PIO Board with ASYST

The board has been tested with and is installable as an 8255.PORT digital device in the ASYST scientific software package by Macmillan Software Company.

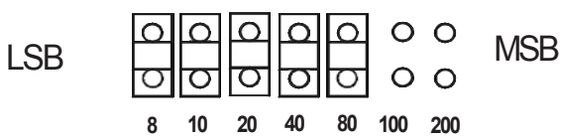
For more details about this package and other PC data acquisition software please contact Blue Chip Technology.

Whilst every effort has been taken to ensure that the information provided is accurate, Blue Chip Technology cannot assume responsibility for any error in this manual or their consequences. Should any errors be detected, the company would greatly appreciate being informed of them. A policy of continuous product development is operated, resulting in the contents of this document being subject to change without notice.

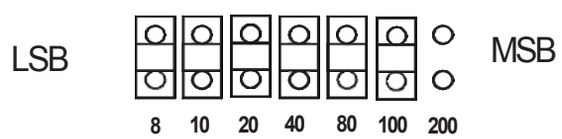
APPENDIX A

Note: View board with back panel on RHS.

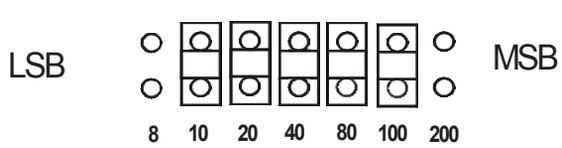
Address Settings for Port 300H



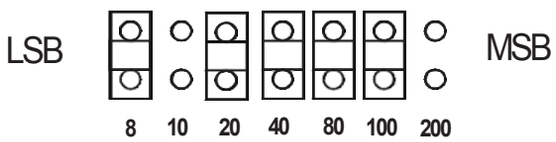
Address Settings for Port 200H



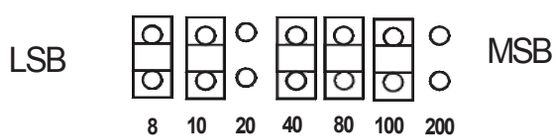
Address Settings for Port 208H



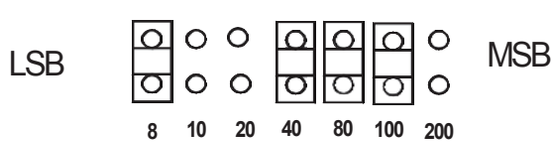
Address Settings for Port 210H



Address Settings for Port 220H



Address Settings for Port 230H



APPENDIX B

PC/XT/AT Port Map
I/O Address Map

Address	
000-01F	DMA Controller 1, 8237A-5
020-03F	Interrupt Controller 1, 8259A
040-05F	Timer, 8254
060-06F	Keyboard Controller, 8742; Control Port B
070-07F	RTC and CMOS RAM, NMI Mask (Write)
080-09F	DMA Page Register (Memory Mapper)
0A0-0BF	Interrupt Controller 2, 8259
0F0	Clear NPX (80287) Busy
0F1	Reset NPX, 80287
0F8-0FF	Numeric Processor Extension, 80287
1F0-1F8	Hard Disk Drive Controller
200-207	Reserved
278-27F	Reserved for Parallel Printer Port 2
2F8-2FF	Reserved for Serial Port 2
300-31F	Reserved
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	Reserved for SDLC Communications, Bisynchronous 2
3A0-3AF	Reserved for Bisynchronous 1
3B0-3BF	Reserved
3C0-3CF	Reserved
3D0-3DF	Display Controller
3F0-3F7	Diskette Drive Controller
3F8-3FF	Serial Port 1

APPENDIX C

PC/XT Interrupt Map

Number	Usage
NMI	Parity
0	Timer
1	Keyboard
2	Reserved
3	Asynchronous Communications
	(Secondary)
	SDLC Communications
4	Asynchronous Communications
	(Primary)
	SDLC Communications
5	Fixed Disk
6	Diskette
7	Parallel Printer

APPENDIX D

AT Interrupt Map

Level		Function
Microprocessor	NMI	Parity or I/O Channel Check
Interrupt Controllers		
CTLR 1	CTLR2	
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Interrupt from CTLR 2
	IRQ 8	Realtime Clock Interrupt
	IRQ 9	Software Redirected to INT 0AH (IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Coprocessor
	IRQ 14	Fixed D isk Controller
	IRQ 15	Reserved
IRQ 3		Serial Port 2
IRQ 4		Serial Port 1
IRQ 5		Parallel Port 2
IRQ 6		Diskette Controller
IRQ 7		Parallel Port 1

APPENDIX F

Application Notes for Interfacing the ISA-PIO

The signals present at ports A, B & C on either the NMOS or CMOS 8255 are TTL (Transistor Transistors Logic) compatible, that is they will interface into standard 74LS logic. However, TTL has limitations when interfacing to other circuitry.

The following should be considered when attempting to interface the ISA-PIO:

1). ISA-PIO cannot drive high capacitances.
2). ISA-PIO cannot sink loads greater than 2.5mA and retain an output voltage that is TTL compatible.
3). ISA-PIO cannot source loads greater than - 200uA (-400uA for CMOS version) and retain an output voltage that is TTL compatible.
4). ISA-PIO cannot interface to any voltage greater than VCC (VDD) + 0.5 or lower than - 0.5V.
5). ISA-PIO cannot drive long lengths of cable into other TTL compatible devices. TTL is a standard for onboard interfacing primarily and is too susceptible to interference and noise to be used with long cable runs.

General TTL requirement:-

LOW	HIGH
Input 0.5 - 0.8V	2.0 - Vcc (VDD)
Output 0 - 0.45V	2.4 - Vcc (VDD)

Characteristics:

DC PARAMETER	SYMBOL	8255 LIMITS MIN	MAX	82C55 LIMITS MIN	MAX
Input Voltage High	VIH	2	VCC	2.2	VDD+0.3V
Input Voltage Low	VIL	-O.5V	0.8V	-0.5V	0.8V
Output Voltage High	VOH	2.4V	@-20uA	3.5	IOH=-400uA
Output Voltage Low	VOL		IOL=1.7MA 0.45V		IOL=2.5MA 0.4V
Input Leakage Current High	ILIH		VI = VCC 10uA		VI = VDD 10uA
Input Leakage Current Low	ILIL		-10uA		VI = 0V -10uA
Output Leakage Current High	ILOH		10uA		VO = VDD 10uA
Output Leakage Current Low	ILOL		-10uA		VO = OV -10uA
Supply Current (Dynamic)	IDDI		120mA		15MA
Supply Current (Standby)	IDD2		120mA	2uA	50uA

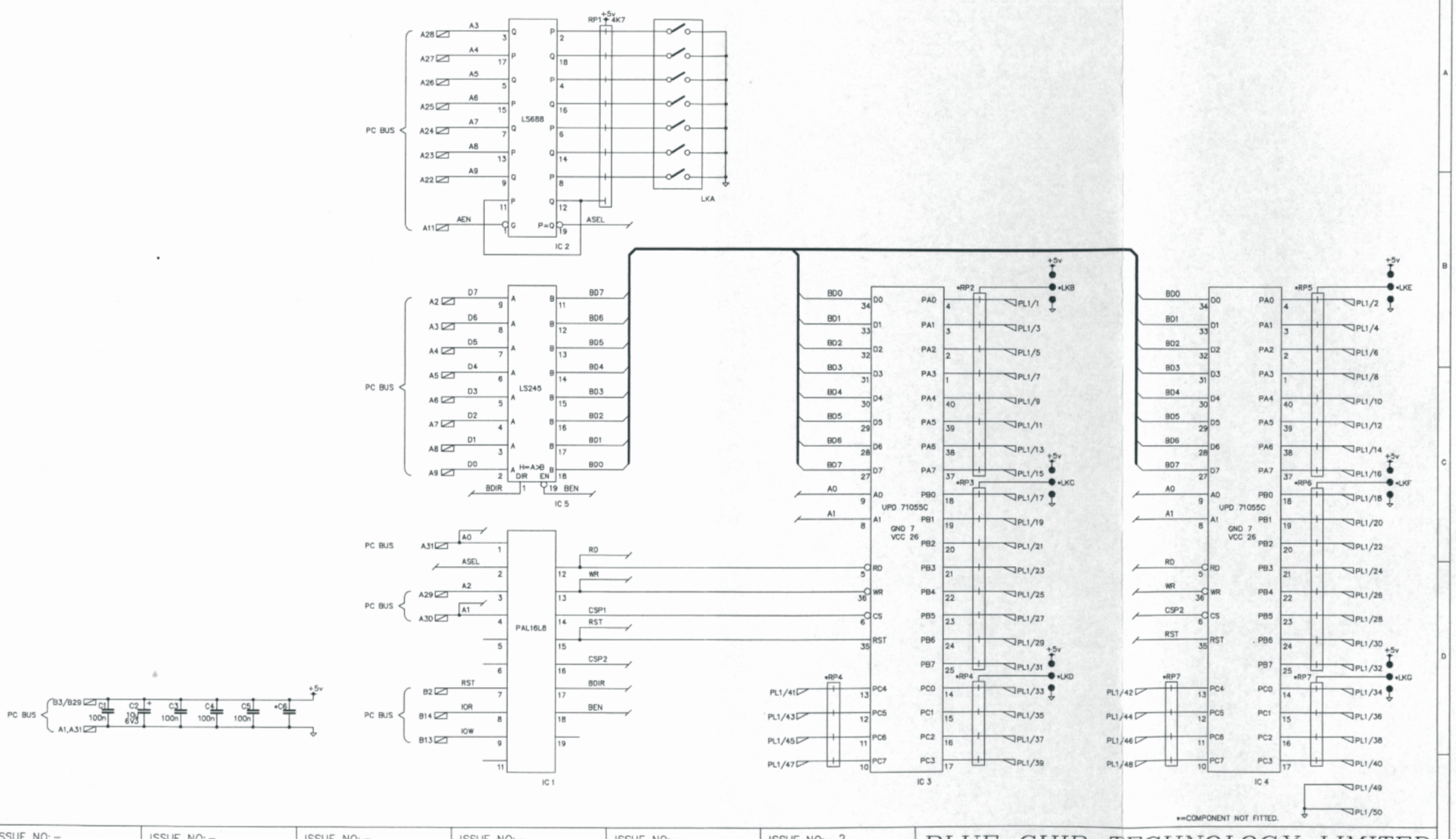
Glossary

VIH - High level input voltage - the minimum and maximum voltages that can be applied (ref to 0V) for a high to be recognised.

VIL - Low level input voltage - the minimum and maximum voltages that can be applied (ref to 0V) for a low to be recognised.

VOH - High level output voltage - the minimum that will be presented at the output as a high at a given max current source current.

VOL - Low level output voltage - the maximum voltage that will be presented at the output as a low at a given maximum current load.



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					GM MMc 18/01/91

BLUE CHIP TECHNOLOGY LIMITED

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SCALE(A3) 0.65	TITLE: 48 CHANNEL PROGRAMMABLE INPUT/OUTPUT MODULE PI048 REV B
CHK'D MMc	
DRAWN S.E.	
DATE: 30/01/87	DRAWING NUMBER: PI048D01 ISS: 2